METHOD FOR FABRICATING MOS SEMICONDUCTOR DEVICE HAVING SALICIDE REGION AND LDD STRUCTURE

FIELD OF THE INVENTION

The present invention relates to a method for fabricating MOS (metal oxide semiconductor) integrated circuit devices, and more particularly to a method for forming salicide regions (self-aligned silicide regions) in a MOS transistor having an LDD (lightly doped drain) structure.

BACKGROUND OF THE INVENTION

In fabrication of MOS devices designed to have feature sizes of 0.35 μm or less, techniques for silicidation of source/drain regions and a polysilicon gate have come into wide use in MOS transistors. Of these techniques, methods for forming a self-aligned silicide region in MOS devices are disclosed in U.S. Pat. Nos. 5,567651 and 5,605,866. These silicidation methods have been employed reduce sheet resistance in an excellent ohmic contact, source/drain region, and polysilicon interconnections; to provide an increased effective contact area; and to provide an etch stopping function.

Other known methods for fabricating MOS devices having a salicide and LDD structure are disclosed in U.S. Pat. Nos. 5,089,865, 5,508,212 and 5,554,549. In these methods, alternative materials such as cobalt, platinum, palladium, nickel, molybdenum or the like are used as salicide materials. Of these salicide materials, particularly, cobalt silicide has lower resistivity in comparison to the other salicide materials, allows low temperature processing, and allows suppression of latch up at an interface of a junction region.

There is a primary known method of forming a MOS transistor having Co-silicide (cobalt silicide) and an LDD structure. In this method, a sidewall spacer formed gate structure is first formed on a semiconductor substrate, and then lightly and heavily doped impurity regions used as source/drain regions are formed by ion implantations using the gate structure as a mask. A layer of cobalt is deposited on an upper polysilicon surface of the gate structure and on an upper surface of the heavily doped impurity region using a chemical vapor deposition process.

Following the cobalt deposition, a first heat treatment, for example, a rapid thermal annealing is carried out at a low temperature in the range of 400° C. to 500° C. to form Co_2Si and CoSi where the cobalt layer is in intimate contact with the silicon or polysilicon regions. After forming the Co_2Si and CoSi compounds a second heat treatment is further carried out at a higher temperature to transform the Co_2Si and CoSi compounds into $CoSi_2$. $CoSi_2$ has a lower resistivity than Co_2Si and CoSi formed in the initial annealing process.

However, under this process of fabricating devices void defects are thereby formed in the cobalt silicide ($CoSi_2$) layer. These voids are generated having a diameter in the range of about 800 Å to 2000 Å. This leads to an increase in junction leakage current of the respective devices. As a result, the conventional MOS transistor having voids in cobalt silicide have deteriorated electrical characteristics.

The following three reasons such void defects are generated in $CoSi_2$ can be observed as evident by using a scanning electron microscope.

(1) An active region of a semiconductor substrate has become damaged during a dry etching process of a very thin (about 50 Å or less) gate insulating layer (for example, a gate oxide layer).

(2) The active region of the semiconductor substrate has become damaged during a dry etching process of forming a gate sidewall spacer.

(3) The active region has become damaged by injecting impurity ions directly into exposed silicon, wherein the impurity ions are accelerated with high energy.

For the above-mentioned reasons, cobalt and silicon atoms at an interface area between the cobalt and silicon layers are locally accelerated or delayed while diffusing by the heat treatment, whereby the void defects are generated.

Herein, we should give attention to the fact that damage of the active region generated due to the above reasons (1) and (2) can be sufficiently prevented by using a higher etch selectivity with respect to the gate oxide layer. The invention is thus provided to solve a problem of void defects caused by the above reason (3), that is, to prevent the active region from becoming damaged during the ion implantation for forming a heavily doped region in the active region.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method for fabricating a MOS integrated circuit device with a salicide (a self-aligned silicide region) and an LDD structure which has a small leakage function.

It is another object of the invention to provide a method for forming a LDD semiconductor device having a salicide region free from voids.

It is an additional object of the invention to provide a method for fabricating a MOS integrated circuit device which can prevent its active region from becoming damaged during ion implantation for forming a heavily doped region in the active region.

According to one aspect of the present invention, a method for fabricating a MOS transistor comprises the steps of forming a buffering layer on an active region, performing an ion injection to form a heavily doped region (source/drain region), and forming a self-aligned silicide region (salicide region) on exposed silicon and on a polysilicon gate. With the above method, when the ion injection is performed to form the source/drain region, impurity ions are injected through the buffering layer into the semiconductor substrate. As a result, the substrate surface, particularly, an upper surface of the source/drain region does not become damaged during the ion injection.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention may be understood and its objects will become apparent to those skilled in the art by reference to the accompanying drawings as follows:

FIGS. 1A through 1F are cross-sectional views showing process steps of a novel method for fabricating a MOSFET according to a first embodiment of the present invention;

FIGS. 2A through 2G are cross-sectional views showing process steps of a novel method for fabricating a MOSFET according to a second embodiment of the present invention; and

FIGS. 3A through 3F are cross-sectional views showing process steps of a novel method for fabricating a MOSFET according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A novel method for fabricating a MOS transistor in accordance with the invention comprises forming a buffer-

ing layer on an active region, performing an ion implantation to form a heavily doped region (source/drain region), and forming a self-aligned silicide region (salicide region) on exposed silicon and on a polysilicon gate. With this method, a salicide region free from voids can be formed because transition metal material (for example, cobalt) and silicon atoms at an interface area between the transition metal layer and the substrate silicon are not locally accelerated or delayed during the formation of the salicide region.

Embodiment 1

FIGS. **1A** through **1F** illustrate a novel method for fabricating a MOSFET according to a first embodiment of the present invention.

Referring to FIG. **1A**, a gate insulating layer **12** of, for example, oxide and a polysilicon gate **13** are sequentially formed on an active region or an n type well of a semiconductor substrate **11**, and are patterned by a photolithography and an etching process. As a result, a gate pattern consisting of the gate oxide layer **12** and the polysilicon gate **13** is formed.

With reference to FIG. **1B**, a phosphorous (or boron) ion implantation into the semiconductor substrate **11** is carried out using the gate pattern as a mask to form an n^- type (or p^- type) impurity region **14** of low concentration on both sides of the gate pattern.

In FIG. **1C**, an insulating layer **15** of, for example, SiO_2 or SiN is deposited over the semiconductor substrate **11** including the gate pattern.

As shown in FIG. **1D**, an anisotropic etch process of the insulating layer **15** is carried out in order to form a sidewall spacer **15***a* on both sidewalls of the gate pattern and in order that a part of the insulating layer **15** remains having a thickness of about 30 Å or more on an upper surface of the polysilicon gate **13** and on the impurity region **14**. Hereinafter, the remaining insulating layer is indicated by a reference numeral **15***b*, and the gate pattern including the sidewall spacer **15***a* is referred to as a gate structure.

Next, as shown again in FIG. **1D**, an arsenic (or BF_2) ion implantation is carried out using the gate structure as a mask to form an n^+ type (or p^+ type) impurity region **17**. As a result, a source/drain **18** is formed which has an LDD (lightly doped drain) structure consisting of the low concentration impurity region (lightly doped source/drain extension) **14** and the high concentration impurity region (source/drain region) **17**. During the ion implantation, the remaining insulating layer **15***b* is used as a buffering layer which is capable of preventing the active region of the semiconductor substrate from becoming damaged.

Referring to FIG. **1E**, after removal of the remaining insulating layer **15***b* on both the upper surfaces of the polysilicon gate **13** and the source/drain region **17**, a magnetic transition metal layer **19** is formed having a thickness of 100 Å to 250 Å (preferably, a thickness of about 150 Å) by PVD (physical vapor deposition) or CVD (chemical vapor deposition) using plasma. The transition metal layer **19** may be made of at least one selected from a group consisting of Co (cobalt), Ti (titanium), Ni (nickel) and the like.

Finally, as shown in FIG. **1F**, an annealing is performed so that a self-aligned silicide layer **20** having a thickness of 400 Å to 800 Å can be formed at both tops of the polysilicon gate **13** and the source/drain region **17** by reaction with the transition metal layer **19**. In this embodiment, the annealing is accomplished by two continuous steps, a low-temperature RTA (rapid thermal annealing) and a high-temperature thermal annealing. Preferably, the low-temperature RTA is performed at a temperature between 400° C. to 500° C., and the high-temperature thermal annealing is performed at a temperature of approximately 650° C. or more.

After formation of the silicide layer **20**, unreacted portions of the transition metal layer **19** are selectively removed, and then metalization is performed as is well-known in the art. As a result, a MOSFET is completely fabricated.

Embodiment 2

FIGS. **2A** through **2G** illustrate a novel method for fabricating a MOSFET according to a second embodiment of the present invention.

Referring to FIG. **2A**, a gate insulating layer **22** of, for example, oxide and a polysilicon gate **23** are sequentially formed on an active region or an n type well of a semiconductor substrate **21**, and are patterned by a photolithography and an etching process. As a result, a gate pattern consisting of the gate oxide layer **22** and the polysilicon gate **23** is formed.

With reference to FIG. **2B**, a phosphorous (or boron) ion implantation into the semiconductor substrate **21** is carried out using the gate pattern as a mask to form an n^- type (or p^- type) impurity region **24** of low concentration on both sides of the gate pattern.

In FIG. **2C**, an insulating layer **25** of, for example, SiO_2 or SiN is deposited over the semiconductor substrate **21** including the gate pattern.

As shown in FIG. **2D**, an anisotropic etch process of the insulating layer **25** is carried out to form a sidewall spacer **25***a* on both sidewalls of the gate pattern, and thereby a gate structure is formed.

Next, as shown again in FIG. **2E**, an insulating layer **26** of, for example, SiO_2 or SiN is formed over the semiconductor substrate including the gate pattern. The insulating layer **26** has a thickness of about 30 Å or more. And, an arsenic (or BF_2) ion implantation, using the gate structure as a mask, is carried out to form an n^+ type (or p^+ type) impurity region **27**. As a result, a source/drain **28** is completely formed which has an LDD (lightly doped drain) structure consisting of the low concentration impurity region (lightly doped source/drain extension) **24** and the high concentration impurity region (source/drain region) **27**. During the ion implantation, the insulating layer **26** is used as a buffering layer which is capable of preventing the active region of the semiconductor substrate from becoming damaged.

Referring to FIG. **2F**, after removal of the insulating layer **26**, a magnetic transition metal layer **29** is formed having a thickness of 100 Å to 250 Å (preferably, a thickness of about 150 Å) by PVD or CVD using plasma. The transition metal layer **29** may be made of at least one selected from a group consisting of Co, Ti, Ni and the like.

Finally, as shown in FIG. **2G**, an annealing is performed so that a self-aligned silicide layer **30** having a thickness of 400 Å to 800 Å can be formed at both tops of the polysilicon gate **23** and the source/drain region **27** by reaction with the transition metal layer **29**.

In this embodiment, the annealing is accomplished by two continuous steps, a low-temperature RTA (rapid thermal annealing) and a high-temperature thermal annealing, which are identically with the first embodiment. Preferably, the low-temperature RTA is performed at a temperature between 400° C. to 500° C., and the high-temperature thermal annealing is performed at a temperature of approximately 650° C. or more.

Subsequently, after formation of the silicide layer **30**, unreacted portions of the transition metal layer **29** are selectively removed, and then metalization is performed as is well-known in the art.